

**HIGH PERFORMANCE SRAM DEVICE AND  
METHOD OF POWERING-DOWN THE SAME**

**ABSTRACT OF THE DISCLOSURE**

An SRAM device and a method of powering-down an SRAM device. In one embodiment, the SRAM device includes (1) an SRAM array coupled to an SRAM array low voltage source that provides a low SRAM array supply voltage  $V_{SB}$  to the SRAM device and (2) main column peripheral circuitry having main pre-charge circuitry free of an SRAM header, coupled to the SRAM array by bit lines and coupled to a sleep mode controller through an associated main column peripheral driving circuitry that is configured to isolate the bit lines from a power supply during a sleep mode.